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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/512,978	02/24/2000	Robert Kerr	MI22-1343	5932

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EXAMINER
CAO, PHAT X

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 01/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/512,978	KERR ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *51-59 and 62-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *51-59 and 62-71* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The cancellation of claims 60-61 in Paper No. 16 is acknowledged.

Claim Rejections - 35 USC § 112

2. Claim 65 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. .

In claim 65, the lateral spacing between adjacent conductive lines substantially equals respective lateral widths of the conductive lines is bot supported by the original disclosure.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 51-54 and 63-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno (US. 5,895,939) in view of Krivokapic et al (US. 6,008,094).

With respect to claims 51 and 63-64, Ueno (Fig. 6) discloses an integrated circuit comprising: a semiconductor substrate 63; a diffusion region 65 formed within the substrate, the diffusion region 65 and substrate 63 forming a junction; a conductive gate line 67 formed over the substrate and diffusion region, a portion of the conductive gate line 67 over the diffusion region 65 comprising an entirely of the lateral width of the conductive gate line 67 received directly over the diffusion region; and wherein the junction is configured to be reverse biased to preclude electrical shorting between the conductive line 67 and the substrate 63 for selected magnitudes of current provided through the conductive line (column 9, lines 65-67 through column 10, lines 1-2).

Ueno does not disclose more than one conductive gate lines having a uniform lateral width and comprising equal lateral spacing between adjacent conductive gate lines.

However, Krivokapic (Fig. 4) teaches the forming of a MOS device comprising a plurality of conductive gate lines L having a uniform lateral width Lg and equal lateral spacing between adjacent conductive gate lines. Accordingly, it would have been obvious to modify Ueno's device by forming more than one conductive gate lines having the structure as set forth above in order to form a logic gate having symmetrical gate regions, as taught by Krivokapic (column 4, lines 43-51).

With respect to claim 65, Krivokapic further teaches the forming of the lateral gate spacing being equal to respective lateral widths of the gate lines for improving the gate delay (column 3, lines 16-19).

With respect to claims 52-54, Ueno's Fig. 6 further discloses the diffusion region 65 comprises two portions disposed outwardly from directly beneath the conductive gate line, a first portion outward of a first side of the conductive line and a second portion outward of a second side of the conductive line.

5. Claims 55-58, 59, 62, and 66-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komatsu et al (US. 4,516,147) in view of Wolf (vol. 3).

With respect to claims 55-57 and 59, Komatsu (Fig. 4) discloses an integrated circuit comprising: a semiconductor substrate having P-type base region 44; an emitter diffusion region 45 of N-type formed within the base region of the substrate, the emitter diffusion region 45 and the base region 44 of the substrate forming a junction; a conductive line 48E formed over the substrate and the diffusion region; a conductive material 49E interconnecting the conductive line 48E and the diffusion region 45, a portion of the conductive material 49E received directly over the conductive line, and an entirety of the portion of the conductive material received directly over the diffusion region; wherein the diffusion region 45 comprises at least two portions disposed outwardly from directly beneath the combined cross-sectional are of the conductive material 49E and the conductive line 48E.

Komatsu does not specifically discloses that the emitter diffusion region and the base region of the substrate forming a reverse biased junction for selected magnitudes of current provided through the conductive line.

However, Wolf teaches the obviousness of using n and p dopants in four different MOSFETs configurations, formation of pn junction and reverse biasing a pn junction of the diffusion region and the substrate by selectively apply magnitudes of voltage provided through the conductive gate line of MOSFET (see Fig. 4-2 on page 137 and related text, on page 136, section 4.1.1). Accordingly, it would have been obvious to form a reverse biased pn junction between the emitter diffusion region and the base region of the substrate for selected magnitudes of voltage on current provided through the conductive base line and the conductive emitter line of Komatsu's transistor because according to Wolf, this is a basis operation of a transistor (i.e., MOS, BJT) when the transistor is in OFF mode.

With respect to claims 66-67 and 69-70, recitation to the conductive line comprising "two conductive layers" fails to distinguish over Komatsu's conductive line 48E, which can be arbitrarily subdivided into numerous sub-layers about each other.

With respect to claims 58 and 62, forming metal for the conductive material of Komatsu would have been obvious because metal is a known material for providing the electrical contacts.

With respect to claims 68 and 71, Komatsu's Fig. 4 further discloses that the conductive material 49E extends on both sides of the conductive line 48E to form sidewall spacers adjacent respective sides of the conductive line 48E.

Response to Arguments

6. Applicant's arguments with respect to the claimed invention have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. This action is made non final.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (703) 308-4917. The Examiner can normally be reached on Monday through Thursday. If attempts to reach the Examiner by telephone are unsuccessfully, the Examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. Group 2800 fax number is (703) 308-7722 or (703) 308-7724.

PHAT X. CAO
PRIMARY EXAMINER

PC
January 12, 2003